IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) Method for fabricating a semiconductor structure having a plurality of gate stacks on a semiconductor substrate, having the following steps:
   (a) ~~application of~~ applying the gate stacks to a gate dielectric above the semiconductor substrate;
   (b) ~~formation of~~ forming a sidewall oxide on sidewalls of the gate stacks;
   (c) ~~application~~ applying and patterning of [[a]] mask on the semiconductor structure; [[and]]
   (d) ~~implantation of~~ implanting a contact doping in a self-aligned manner with respect to the sidewall oxide of the gate stacks in regions not covered by the mask; and
   (e) after implanting the contact doping, reducing the sidewall oxide in its lateral extent in regions not covered by the mask for resulting in a thinned sidewall oxide.
2. (Canceled)
3. (Currently Amended) Method according to claim [[2]] 1, wherein the reduction of the extent of the lateral sidewall oxide for resulting in a thinned side wall oxide is followed by a further implantation of different doping.
4. (Previously Presented) Method according to claim 3, wherein the further doping is a p-type doping having a low concentration, preferably with a dopant concentration that is at least a power of ten lower than the contact doping concentration.
5. (Currently Amended) Method according to claim 3, wherein the further doping is a bit line halo doping implanted from a predetermined direction at a predetermined angle α, preferably in the range of between about 0° and 30° inclusive.

6. (Previously Presented) Method according to claim 1, wherein the contact doping is implanted at a predetermined angle of $\alpha = 0°$.

7. (Previously Presented) Method according to claim 1, wherein the contact doping is an n-type doping having a high concentration, for example having an implantation dose of about 10^{14} to $3 \cdot 10^{15}/cm^2$, preferably with arsenic.

8. (Previously Presented) Method according to claim 1, wherein a removal of the mask is followed by an implantation of a, preferably identical, dopant having a lower dopant concentration than that of the contact doping.

9. (Previously Presented) Method according to claim 1, wherein the gate stacks are applied approximately equidistantly with respect to one another, a storage capacitor being arranged alternately below every third or first adjacent gate in the semiconductor substrate in a cross-sectional plane.

10. (Previously Presented) Method according to claim 1, wherein the method is used for fabricating logic transistors.

11. (Previously Presented) Method according to claim 1, wherein the method is used for fabricating selection transistors, preferably of a DRAM.

12. (Previously Presented) Method according to claim 1, wherein the gate stacks are fabricated with a length of less than 200 nm.

13. (Previously Presented) Method according to claim 1, wherein the gate stacks are provided parallel and in strip-type fashion on the semiconductor substrate.

14. (Previously Presented) Method according to claim 1, wherein the gate stacks have a lower first layer made of polysilicon and an overlying second layer made of a metal silicide or a metal.

15. (Previously Presented) Method according to claim 1, wherein the gate stacks are created by carrying out an application and patterning of the first layer, the overlying second layer and a third layer arranged thereon on the gate dielectric.

16. (Previously Presented) Method according to claim 15, wherein the third layer has silicon nitride or oxide.

IN THE DRAWINGS:

The attached sheet of drawings includes a proposed change to Figure 3. Figure 3 on the drawing sheet has been designated "PRIOR ART". Upon approval by the Examiner, formal drawing sheets will be promptly forwarded.